ABSTRACT OF THE DISCLOSURE

A method and apparatus for inserting design-for-debug (DFD) circuitries in an integrated circuit to debug or diagnose DFT modules, including scan cores, memory BIST (built-in self-test) cores, logic BIST cores, and functional cores. The invention further comprises using a DFD controller for executing a plurality of DFD commands to debug or diagnosis the DFT modules embedded with the DFD circuitries. When used alone or combined together, these DFD commands will detect or locate physical failures in the DFT modules in the integrated circuit on an evaluation board or system using a low-cost DFT debugger. A computer-aided design (CAD) method is further developed to synthesize the DFD controller and DFD circuitries according to the IEEE 1149.1 Boundary-scan Std. The DFD controller supports, but is not limited to, the following DFD commands: RUN_SCAN, RUN_MBIST, RUN_LBIST, DBG_SCAN, DBG_MBIST, DBG_LBIST, DBG_FUNCTION, SELECT, SHIFT, SHIFT_CHAIN, CAPTURE, RESET, BREAK, RUN, STEP, and STOP.